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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,813	SPRUNT ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7-9,18,20,21 and 27-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7-9,18,20,21 and 27-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response and amendment filed on November 2, 2004 has been fully considered. Claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 remain pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

3. Applicant contends that Larsen does not teach or reasonably suggest sending an event detection signal to the multiplexer, and having an event register to instruct the multiplexer to select an event from the list of events by filtering the events that are not to be counted by qualifying a single event that is to be counted (Applicant's remarks, page 9, last paragraph).

However, Larsen expressly discloses sending event occurrences to multiplexer 82 (see, for example, column 5, lines 7-9). The event occurrences are "detected" event occurrences (see, for example, column 6, lines 42-43), or in other words, event detection signals. Therefore, Larson discloses sending an event detection signal to the multiplexer.

Larsen further discloses control registers 80, or in other words, event registers, for instructing the multiplexer to select events (see, for example, column 5, lines 9-17). The events are from a list of events that includes IU, FX, FP, SC, BIU, LB and L2 events (see, for example, column 4, lines 50-57). Therefore, Larson also discloses having an event register to instruct the multiplexer to select an event from the list of events.

Furthermore, Larsen discloses that the control registers (i.e., the event registers) specify the events, if any, to be recorded by a counter (see, for example, column 5, lines 13-17). In other words, some events are counted and some are not counted, which is to say that some events are

selected and other events are filtered and not counted. Therefore, Larsen also discloses selecting an event by filtering the events that are not to be counted.

Larsen further discloses selecting and routing an event to a counter based on the identity of the thread to which the event corresponds (see, for example, column 6, line 54 to column 7, line 3). In other words, events are qualified based on the identity of the thread. Therefore, Larsen also discloses selecting an event by qualifying a single event that is to be counted.

Claim Objections

4. The objection to claim 33 set forth in the previous Office action is withdrawn in view of the amendment.

5. Claim 32 (currently amended) is objected to because of the following informalities: The claim recites "An system," rather than --A system--. Additionally, the new limitation, "by selecting those events that are not to be counted," was perhaps intended to read, --by filtering those events that are not to be counted--, as is now recited in claims 1, 18 and 40 (emphasis provided). Appropriate correction or clarification is required.

Claim Rejections - 35 USC § 112

6. The rejection of claims 2-4, 7 and 8 under 35 U.S.C. 112, second paragraph, as set forth in the previous Office action, is withdrawn in view of the amendment.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3, 7-9, 18, 20, 21, 27-34 and 36-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,835,705 to Larsen et al. (art of record, "Larsen") in view of U.S. Pat. No. 5,657,253 to Dreyer et al. (art of record, "Dreyer").

With respect to claim 1 (currently amended), Larsen discloses an apparatus comprising:

(a) a processor to execute a plurality of threads simultaneously, each thread including a series of instructions (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) an event detector to detect a predetermined list of events and to transmit an event detection signal to a multiplexer (see, for example, performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a predetermined list of events, and column 5, lines 7-9, which shows transmitting the event detection signals to the multiplexer); and

(c) an event register to instruct the multiplexer to select an event from the predetermined list of events by filtering those events that are not to be counted and by qualifying the event that is to be counted based on a set of conditions (see, for example, control registers 80 in FIG. 2, and column 5, lines 9-17, which shows the control registers, i.e. the event registers, selecting events to be counted while filtering other events not to be counted, and qualifying the events based on the mode of operation and other conditions), wherein the qualifying of the event is performed

using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see, for example, column 6, line 54 to column 7, line 3, which shows selecting and routing an event to a counter based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred).

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID, as presented above, Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread current privilege level (CPL).

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen also discloses:

(d) an event counter to count the qualified event (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer).

With respect to claim 3 (currently amended), the rejection of claim 1 is incorporated, and further, Larsen also discloses the limitation wherein the event register comprises a first field of bits to choose the event to be counted (see, for example, column 5, lines 7-17, which shows the control or event registers having bit fields to select the events to be counted).

With respect to claim 7 (previously presented), the rejection of claim 1 is incorporated, and further, although Larsen discloses software-writable event counters (see, for example, column 4, lines 50-57), Larsen does not expressly disclose the limitation wherein the event counter is stopped and cleared before a new event is selected.

However, Dreyer further discloses resetting, i.e. stopping and clearing, the event counter using an instruction (see, for example, column 3, lines 19-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter reset feature taught by Dreyer, for the purpose of stopping and clearing the counter values in software.

With respect to claim 8 (previously presented), the rejection of claim 7 is incorporated, and further, although Larsen discloses software-writable event counters (see, for example, column 4, lines 50-57), Larsen does not expressly disclose the limitation wherein the event counter is preset to a certain state.

However, Dreyer further discloses presetting the event counter to a certain value or state (see, for example, column 3, lines 19-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter preset feature taught by Dreyer, for the purpose of enabling functions such as countdowns (see, for example, Dreyer, column 4, lines 21-30).

With respect to claim 9 (previously presented), the rejection of claim 1 is incorporated, and further, Larsen also discloses the limitation wherein the predetermined list of events includes

hardware performance and breakpoint events (see, for example, column 5, lines 46-56, which shows the predetermined list of events, including hardware performance events such as instructions completed and processor cycles, along with breakpoint events such as thread switch counts).

With respect to claim 18 (currently amended), Larsen discloses a method comprising:

(a) executing a plurality of threads simultaneously, each thread including a series of instructions (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) detecting a predetermined list of events and transmitting an event detection signal to a multiplexer (see, for example, performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a predetermined list of events, and column 5, lines 7-9, which shows transmitting the event detection signals to the multiplexer);

(c) instructing the multiplexer to select an event from the predetermined list of events by filtering those events that are not to be counted and by qualifying the event that is to be counted based on a set of conditions (see, for example, control registers 80 in FIG. 2, and column 5, lines 9-17, which shows the control registers, i.e. the event registers, selecting events to be counted while filtering other events not to be counted, and qualifying the events based on the mode of operation and other conditions), wherein the qualifying of the event is performed using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see, for example, column 6, line 54 to column 7, line 3, which

shows selecting and routing an event to a counter based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred).

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID, as presented above, Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread CPL.

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen also discloses:

(d) counting the event qualified by the multiplexer using an event counter (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(e) accessing the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 20 (previously presented), the rejection of claim 18 is incorporated, and further, Larsen also discloses the limitation wherein the qualifying of the event includes

requiring that the event has a preselected thread ID (see, for example, column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which they correspond).

With respect to claim 21 (previously presented), the rejection of claim 20 is incorporated, and further, Dreyer further discloses the limitation wherein the qualifying of the event further includes requiring that the event has a preselected thread CPL (see, for example, column 4, lines 39-46, which shows control register bits for enabling event counting based on the current privilege level).

With respect to claim 27 (previously presented), the rejection of claim 18 is incorporated, and further, Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for example, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 28 (previously presented), the rejection of claim 20 is incorporated, and further, Larsen also discloses the limitation wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred (see, for example, column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which they correspond).

With respect to claim 29 (previously presented), the rejection of claim 21 is incorporated, and further, Dreyer further discloses the limitation wherein thread CPL indicates a privilege level

at which the thread was operating at when the event occurred (see, for example, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 30 (previously presented), the rejection of claim 1 is incorporated, and further, Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for example, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 31 (previously presented), the rejection of claim 1 is incorporated, and further, Larsen also discloses:

(a) an event counter to count the event qualified by the multiplexer (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(b) an access location to allow access to the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 32 (currently amended), Larsen discloses a system comprising:

(a) a storage medium coupled with a processor (see, for example, main memory 52 and processor 10 in FIG. 1), the processor to execute a plurality of threads simultaneously, each thread including a series of instructions (see, for example, column 3, lines 39-55, which shows

the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) an event detector to detect a predetermined list of events and to transmit an event detection signal to a multiplexer (see, for example, performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a predetermined list of events, and column 5, lines 7-9, which shows transmitting the event detection signals to the multiplexer); and

(c) an event register to instruct the multiplexer to select an event from the predetermined list of events by selecting those events that are not to be counted and by qualifying the event that is to be counted based on a set of conditions (see, for example, control registers 80 in FIG. 2, and column 5, lines 9-17, which shows the control registers, i.e. the event registers, selecting events to be counted while filtering other events not to be counted, and qualifying the events based on the mode of operation and other conditions), wherein the qualifying of the event is performed using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see, for example, column 6, line 54 to column 7, line 3, which shows selecting and routing an event to a counter based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred).

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID, as presented above, Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread CPL.

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen also discloses:

(d) an event counter to count the event qualified by the multiplexer (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(e) an access location to allow access to the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 33 (currently amended), the rejection of claim 32 is incorporated, and further, Larsen also discloses the limitation wherein the access location allows access to determine the count without disturbing the operation of event counter (see, for example, column 7, lines 40-52, which shows accessing the registers to read the count without disturbing the operation of the counters).

With respect to claim 34 (currently amended), the rejection of claim 33 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 3 (see the reasoning applied to claim 3 above).

With respect to claim 36 (previously presented), the rejection of claim 32 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 7 (see the reasoning applied to claim 7 above).

With respect to claim 37 (previously presented), the rejection of claim 36 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 8 (see the reasoning applied to claim 8 above).

With respect to claim 38 (previously presented), the rejection of claim 32 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 9 (see the reasoning applied to claim 9 above).

With respect to claim 39 (previously presented), the rejection of claim 32 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 30 (see the reasoning applied to claim 30 above).

With respect to claim 40 (currently amended), Larsen discloses a machine-readable medium having stored thereon data representing sets of instructions (see, for example, column 3, lines 11-19, which shows a machine-readable medium having instructions stored thereon) the sets of instructions which, when executed by a machine (see, for example, column 4, lines 25-28, which shows executing the instructions), cause the machine to:

(a) execute a plurality of threads simultaneously, each thread including a series of instructions (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) detect a predetermined list of events and transmitting an event detection signal to a multiplexer (see, for example, performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a predetermined list of events, and column 5, lines 7-9, which shows transmitting the event detection signals to the multiplexer);

(c) instruct the multiplexer to select an event from the predetermined list of events by filtering those events that are not to be counted and by qualifying the event that is to be counted based on a set of conditions (see, for example, control registers 80 in FIG. 2, and column 5, lines 9-17, which shows the control registers, i.e. the event registers, selecting events to be counted while filtering other events not to be counted, and qualifying the events based on the mode of operation and other conditions), wherein the qualifying of the event is performed using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see, for example, column 6, line 54 to column 7, line 3, which shows selecting and routing an event to a counter based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred);

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID, as presented above, Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread CPL.

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see, for example, column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen also discloses:

(d) count the event qualified by the multiplexer using an event counter (see, for example, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(e) access the event counter to determine a current count of the event (see, for example, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 41 (previously presented), the rejection of claim 40 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 20 (see the reasoning applied to claim 20 above).

With respect to claim 42 (previously presented), the rejection of claim 41 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 21 (see the reasoning applied to claim 21 above).

With respect to claim 43 (previously presented), the rejection of claim 40 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 27 (see the reasoning applied to claim 27 above).

With respect to claim 44 (previously presented), the rejection of claim 40 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 28 (see the reasoning applied to claim 28 above).

With respect to claim 45 (previously presented), the rejection of claim 41 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 29 (see the reasoning applied to claim 29 above).

9. Claims 4 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen in view of Dreyer, as applied to claims 1 and 34 above, respectively, and further in view of U.S. Pat. No. 6,205,468 to Diepstraten et al. (art of record, "Diepstraten").

With respect to claim 4 (currently amended), the rejection of claim 1 is incorporated, and further, although Larsen discloses control or event registers having bit fields for selecting the events to be recorded, setting the mode of operation, and enabling or disabling event counting (see, for example, column 5, lines 7-17), Larsen does not expressly disclose the limitation

wherein the event register further comprises a second field of bits to choose the event to be masked and not counted.

However, Diepstraten discloses an event masker associated with an event recorder that includes control bits for masking events (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50, which shows masking events to select one or more events to be ignored, i.e. not counted).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the event masking feature taught by Diepstraten, for the purpose of reducing the number of events that will be processed (see, for example, Diepstraten, column 4, lines 42-50).

With respect to claim 35 (currently amended), the rejection of claim 34 is incorporated, and further, the limitations recited in the claim are analogous to those of claim 4 (see the reasoning applied to claim 4 above).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2192

mjy

WEI Y. ZHEN
PRIMARY EXAMINER